In the claims:

For the Examiner's convenience, all pending claims are presented below with changes shown.

1. (Previously Presented) A computer system comprising:

a processor including:

a central processing unit (CPU) core to execute non-graphic instructions;

a graphics core to compute graphical transformations via supersampling techniques; and

a unified graphics cache coupled to the graphics core to store a supersampled image.

2. (Original) The computer system of claim 1 wherein the graphics cache comprises:

a texture cache to store texture data; and

a color and depth buffer to store the color data and the depth data.

3. (Previously Presented) The computer system of claim 1 further comprising:

a CPU cache coupled to the CPU core.

4. (Original) The computer system of claim 3 further comprising a bus interface coupled to the CPU cache and the graphics cache.

5. (Previously Presented) The computer system of claim 1 wherein the graphics core performs rendering according to a tile-based rendering architecture.

6. (Previously Presented) The computer system of claim 1 further comprising:

a bus interface coupled to CPU cache and the graphics cache; and

a main memory coupled to the bus interface.

7. (Original) The computer system of claim 2 wherein the graphics core amplifies image polygons and renders the polygons into the graphics cache.

8. (Previously Presented) The computer system of claim 7 wherein amplification of the image polygons are implemented via viewport transformation.

9. (Original) The computer system of claim 7 wherein the graphics core downsamples the image polygons after the polygons have been rendered.

10. (Original) The computer system of claim 9 wherein the downsampling of the image polygons are implemented by executing a bit aligned block transfer.

11. (Currently Amended) A method for supersampling an image comprising:

receiving polygons of a first tile of the image at a graphics core; ~~and~~

amplifying the polygons at the graphics core; and

rendering the polygons of the first tile into a unified graphics cache, wherein the unified graphics cache stores texture data, color data and depth data of the image.

12. (Previously Presented) The method of claim 11 further comprising executing a stretch aligned block transfer at the graphics core after rendering the polygons.

13. (Previously Presented) The method of claim 11 wherein the polygons are amplified four times the original size of the image.

14. (Previously Presented) The method of claim 11 wherein the amplification is achieved using viewport transformation.

15. (Original) The method of claim 11 wherein the process of rendering the polygons comprises:

setting up the image polygons; and

rasterizing pixels within the image polygons.

16. (Original) The method of claim 15 further comprising texturing the pixels within the image polygons.

17. (Original) The method of claim 11 further comprising downsampling the polygons after the polygons have been rendered.

18. (Original) The method of claim 17 wherein the downsampling is achieved by executing a bit aligned block transfer.

19. (Original) The method of claim 11 further comprising:

determining whether the unified graphics cache includes more tiles that are to be rendered; and

if so, receiving polygons of a second tile of the image at the graphics core; and rendering the polygons of the second tile into the unified graphics cache.

20. (Previously Presented) A central processing unit (CPU) comprising:

a CPU core to execute non-graphic instructions;

CPU cache coupled to the CPU core;

a graphics accelerator to compute graphical transformations via supersampling techniques; and

a unified graphics cache coupled to the graphics core and the CPU, to store a supersampled image.

21. (Original) The CPU of claim 20 wherein the graphics cache comprises:

a texture cache to store texture data; and

a color and depth buffer to store the color data and the depth data.

22. (Previously Presented) The CPU of claim 20 wherein the graphics core amplifies image polygons and renders the polygons into the graphics cache.

23. (Original) The CPU of claim 22 further comprising a bus interface coupled to the CPU cache and the graphics cache.

24. (Previously Presented) The CPU of claim 23 wherein the graphics accelerator performs rendering according to a tile-based rendering architecture.